

TITLE

MEHTOD OF PROCESSING SIGNAL OF LCM TIMING CONTROLLER

5

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates in general to a method of processing signals. In particular, the present invention relates to a method of processing signals of an LCM(LCD Module, Liquid Crystal Display Module) timing controller.

Description of the Related Art

According to U.S. Patent No.5856818, as shown in Fig.1, an LCM 10 has a timing controller 12 which generates signals, such as a gate clock signal CPV, start vertical signals STV1,STV2, or a gate-on enable signal OE for a gate driver 16 and a source driver 18 of a LCD panel 14 after receiving a horizontal synchronizing signal HSYNC, a vertical synchronizing signal VSYNC, and a data enable signal DE.

In another mode, as shown in Fig.2, the timing controller 12 which generates signals, such as a gate clock signal CPV, start vertical signals STV1,STV2, or a gate-on enable signal OE for a gate driver 16 and a source driver 18 of a LCD panel 14 after receiving a data enable signal DE.

In the method of processing signals of a conventional timing controller, as shown in Fig.3 or Fig.4, a next control signal is generated according to a memory value of a previous horizontal or vertical cycle. When an LCD module is in DE mode

or in the mode of three synchronizing signals HSYNC, VSYNC, DE,
a conventional timing controller decodes control signals
according to the memory values of horizontal and vertical
cycles. For example, in a vertical blank period VB (v-blank)
5 of the data enable signal DE, the start vertical signals
STV1,STV2 are generated according to the gate clock signal CPV.

Refer to Fig.5 and Fig.6 which correspond to the methods
of processing signals in Fig.3 and Fig.4 respectively. The
timing controller processes signals according to the memory
10 values of horizontal and vertical cycles, such as the vertical
blank period VB (v-blank), the gate clock signal CPV. Since
signals of the horizontal and vertical cycles are unstable, the
horizontal or vertical cycle of a video signal is caused to vary.
As far as the timing controller is concerned, the cycle variance
15 incurs erroneous operations of control signals. For example, the
gate clock signal CPV does not generate the start vertical
signals STV1,STV2 until after the vertical blank period
VB(v-blank) of the data enable signal DE, and the display frame
of the LCD module is therefore caused to jitter or bounce. The
20 start vertical signals STV include: a first start vertical
signal STV1, for determining a start scan location of a frame;
and a second start vertical signal STV2, for offsetting the
flicker and display brightness.

25 SUMMARY OF THE INVENTION

Accordingly, an object of the present invention provides a
solution to the problem caused by a conventional timing
controller which processes signals according to a memory value
of a previous horizontal or vertical cycle. The present
30 invention provides a real time process, instead of the process

of using a cycle memory value, so as to process control signals in real time, thereby acquiring a correct control waveform which drives the LCD module.

5 The real time process for control signals can overcome the timing controller's erroneous operations caused by cycle variance. Basically, in DE mode, instead of the horizontal and vertical cycle values, the vertical synchronizing signal generated from decoding the DE signal is used as a reference basis. Signals are processed at the rising edge or the falling edge of a vertical synchronizing signal, and the control signals of the LCD module are generated in real time. For example, after the start vertical signals STV1,STV2 and the gate-on enable signal OE are generated in real time, the CPV (gate clock signal), STV1,STV2, and OE pause to be outputted till the timing controller detects a first DE signal after the vertical blank period, and then the normal control signals restart to be outputted, so that the real time driving is achieved.

15 If the timing controller receives the synchronizing signals DE, HSYNC, and VSYNC from outside simultaneously, the control signals are generated according to HSYNC and VSYNC. HSYNC resets each horizontal cycle. VSYNC, same as in DE mode, generates the control signals of LCD module at the rising edge or the falling edge of VSYNC. After the control signals corresponding to a timing sequence are outputted, the control signals CPV, STV1, STV2, and OE pause to be outputted (the process is the same as in DE mode).

BRIEF DESCRIPTION OF THE DRAWINGS

20 The present invention can be more fully understood by reading the subsequent detailed description in conjunction with

the examples and references made to the accompanying drawings,
wherein:

Fig. 1 is a schematic diagram of a LCD module which receives
three synchronizing signals DE, HSYNC, VSYNC simultaneously;

5 Fig. 2 is a schematic diagram of a LCD module in DE mode;

Fig. 3 shows a timing diagram of the signals of a
conventional LCD module receiving DE, HSYNC, VSYNC
simultaneously;

10 Fig. 4 shows a timing diagram of the signals of a
conventional LCD module in DE mode;

Fig. 5 shows a timing diagram of the signals of a
conventional LCD module which, receiving DE, HSYNC, VSYNC
simultaneously, does not operate properly;

15 Fig. 6 shows a timing diagram of the signals of a
conventional LCD module which does not operate properly in DE
mode;

Fig. 7 shows a timing diagram of the signals of an LCD module
receiving DE, HSYNC, VSYNC simultaneously in accordance with a
preferred embodiment of the present invention; and

20 Fig. 8 shows a timing diagram of the signals of an LCD module
in DE mode in accordance with a preferred embodiment of the
present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

25 Refer to Fig.7 and Fig.8. To solve the problems caused by
a conventional timing controller which processes signals
according to the cycle memory values, the present invention
provides a real time process, in stead of the process of using
cycle memory values, so as to process control signals in real

time, thereby acquiring a correct control waveform which drives the LCD module.

Refer to Fig.2 and Fig.8. In DE mode, the vertical synchronizing signal generated from decoding the signal DE, instead of the vertical blank period VB(v-blank) and gate clock signal CPV, is used as a reference basis. Signals are processed at the rising edge or the falling edge of a vertical synchronizing signal, and the control signals of the LCD module 10 are generated in real time. For example, after the start vertical signals STV1, STV2 and the gate-on enable signal OE are generated in real time, the CPV (gate clock signal), STV1, STV2, and OE pause to be outputted till the timing controller 12 detects a first DE signal after the vertical blanking period, and then the normal control signals restart to be outputted so that the real time driving is achieved.

Refer to Fig.1 and Fig.7. If the timing controller 12 receives the synchronizing signals DE, HSYNC, and VSYNC from outside simultaneously, the control signals are generated according to HSYNC and VSYNC. HSYNC resets each horizontal cycle. VSYNC, same as in DE mode, generates the control signals of LCD module 10 at the rising edge or the falling edge of VSYNC. After the control signals corresponding to a timing sequence are outputted, the control signals CPV, STV1, STV2, and OE pause to be outputted (the process is the same as in DE mode).

To solve the problem caused by a conventional timing controller which processes signals according to a vertical blank period VB(v-blank) and a gate clock signal CPV, the present invention provides a method of processing signals of a timing controller 12 of the LCD module 10, the method includes the steps of: at first, the timing controller 12 receives a data enable

signal DE which has a vertical blank period VB; the timer
controller 12 generates a gate clock signal CPV which has a
plurality of gate clock cycles C1-Cn; then, the timing
controller 12 generates a plurality of gate-on enable signals
5 OE simultaneously according to the plurality of gate clock
cycles C1-Cn of the gate clock signal CPV; then, before the end
of the vertical blank period VB and after at least a gate clock
cycle C1 during the vertical blank period VB, start vertical
signals STV(including STV1 and STV2) are generated; and, the
10 timing controller 12 pauses outputting CPV, STV(including STV1
and STV2), and OE till the end of the vertical blank period VB.

Finally, while the invention has been described by way of
example and in terms of the preferred embodiment, it is to be
understood that the invention is not limited to the disclosed
15 embodiments. On the contrary, it is intended to cover various
modifications and similar arrangements as would be apparent to
those skilled in the art. Therefore, the scope of the appended
claims should be accorded the broadest interpretation so as to
encompass all such modifications and similar arrangements.